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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,760	12/27/2001	Byoung Ho Lim	049128-5053	9786
30827	7590	11/01/2005	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			LANDAU, MATTHEW C	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/026,760	Applicant(s) LIM, BYOUNG HO	
	Examiner Matthew Landau	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-10,12-14 and 16-21 is/are rejected.
- 7) ☒ Claim(s) 2,11 and 15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 10, 13, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin (US Pat. 5,766,493).

Regarding claims 1, 10, 13, and 21, Figures 3A-3E of Shin disclose a method of fabricating a liquid crystal display panel comprising the steps of: preparing an upper substrate 20 and a lower substrate 10; bonding the upper substrate to the lower substrate; cleaning exposed surfaces of the bonded upper and lower substrates to removed foreign materials formed on the lower substrate during the preparing of the lower substrate; and simultaneously eliminating the cleaned exposed surfaces of the bonded upper and lower substrates, wherein a thickness of the panel is uniformly reduced. Note that Shin's disclosed step of preparing the lower substrate (including forming a TFT, pixel electrode, scanning line and data line) (col. 3, lines 53-57) will result in at least some type of impurity/foreign material adhering to the exposed surface of the lower substrate 10. Shin discloses immersing the bonded substrates in a liquid etchant to reduce the thickness of the substrates (col. 4, lines 14-20). Since the substrates are bonded prior to etching, the exposed surfaces are eliminated simultaneously and the thickness is reduced uniformly. It is inherent that at least some of the foreign materials on the lower substrate will be removed when the bonded upper and lower substrates are dipped in the etchant bath due to

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contact with the liquid. If for some reason there is not at least some foreign materials removed upon contact with the liquid etchant, it is inherent that at least some foreign materials are removed when the surface upon which they are adhered is etched away. Therefore, it can be considered that the surfaces of the substrates are first cleaned and then eliminated.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3-10, 12-14, and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Matsushima.

Regarding claims 1, 3, 10, 12-14, 16, 20, and 21, Figures 2A-F and Figure 3 of this instant application discloses a method of fabricating a liquid crystal display panel, comprising the steps of: preparing an upper substrate 28 and a lower substrate 18; forming a gate electrode 15 on the lower substrate 18; forming a gate insulating film 19 on the lower substrate to cover the gate electrode; forming an active layer 21 on the gate insulating film; and forming a source electrode 13 and a drain electrode 11 on the active layer; and bonding an upper substrate 28 to a lower substrate 18. Figure 3 of the APA also discloses foreign materials 25A formed on the lower substrate during the preparing of the lower substrate. The difference between the APA and the claimed invention is the steps of cleaning the exposed surfaces of the bonded upper and

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lower substrates to remove the foreign materials and simultaneously eliminating/removing the cleaned exposed surfaces of the bonded upper and lower substrates. Matsushima discloses a method of fabricating an LCD panel including wet-etching the exposed surfaces of bonded upper and lower substrates (100a and 101a, respectively) (col. 8, lines 26-36). Furthermore, since the upper and lower substrates (100a and 101a, respectively) are bonded prior to be immersed in an etching tank, exposed surfaces of both substrates are eliminated simultaneously and the thickness of the LCD panel is reduced uniformly. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of the APA by using the etching process of Matsushima for the purpose of reducing the total weight of the substrates and obtaining a smooth surface. Note that it is inherent that at least some of the foreign materials on the lower substrate will be removed when the bonded upper and lower substrates are dipped in the etchant bath due to contact with the liquid. If for some reason there is not at least some foreign materials removed by the liquid etchant, it is inherent that at least some foreign materials are removed when the surface upon which they are adhered is etched away. Therefore, it can be considered that the surfaces of the substrates are first cleaned and then eliminated.

Regarding claim 4, Figures 2A-2F of the instant application disclose the steps of: forming a thin film transistor on the lower substrate 18; forming a protective layer 25 on the lower substrate; and forming a pixel electrode 12 on the protective layer to electrically contact the thin film transistor.

Regarding claim 5, the APA discloses the pixel electrode 12 is formed of indium-tin-oxide (page 5, para. [0013] of the instant application).

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Regarding claim 6, the APA discloses the protective layer 25 is formed of an acrylic organic compound (page 5, para [0011]).

Regarding claim 7, Figures 2A-2C of the instant application disclose the step of forming the thin film transistor includes: forming a gate electrode 15 on the lower substrate 18; forming a gate insulating film 19 on the lower substrate to cover the gate electrode; forming an active layer 21 on the gate insulating film; and forming a source electrode 13 and a drain electrode 11 on the active layer.

Regarding claim 8, Figure 2C of the instant application discloses the source electrode 13 and drain electrode 11 contact the gate insulating film.

Regarding claim 9, Figure 2F of the instant application discloses the pixel electrode 12 contacts parallel and inclined surfaces of the drain electrode 11.

Regarding claim 17, Figures 2D-2F of the instant application disclose the steps of: forming a protective layer 25 on the lower substrate; and forming a pixel electrode 12 on the protective layer to electrically contact the drain electrode 11.

Regarding claim 18, the APA discloses the pixel electrode 12 is formed of indium-tin-oxide (page 5, para. [0013] of the instant application).

Regarding claim 19, the APA discloses the protective layer 25 is formed of an acrylic organic compound (page 5, para [0011]).

Claims 1, 3-10, 12-14, and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the APA in view of Doh (US Pat. 6,675,817).

Regarding claims 1, 3, 10, 12-14, 16, 20, and 21, Figures 2A-F and Figure 3 of this instant application discloses a method of fabricating a liquid crystal display panel, comprising the steps of: preparing an upper substrate 28 and a lower substrate 18; forming a gate electrode 15 on the lower substrate 18; forming a gate insulating film 19 on the lower substrate to cover the gate electrode; forming an active layer 21 on the gate insulating film; and forming a source electrode 13 and a drain electrode 11 on the active layer; and bonding an upper substrate 28 to a lower substrate 18. Figure 3 of the APA also discloses foreign materials 25A formed on the lower substrate during the preparing of the lower substrate, and more specifically, during the formation of a protective layer on the lower substrate (paragraph [0011] of the instant application). The difference between the APA and the claimed invention is the steps of cleaning the exposed surfaces of the bonded upper and lower substrates to remove the foreign materials and simultaneously eliminating/removing the cleaned exposed surfaces of the bonded upper and lower substrates. Doh discloses a method of removing impurities from a substrate 219 (col. 4, lines 13-18). Doh also discloses uniformly reducing the thickness (eliminating exposed surfaces) of the glass substrate by immersing in a liquid etchant bath (col. 4, lines 39-44). It can be considered that the impurities are removed prior to the step of eliminating exposed surfaces since the removal/etching process continues after the removal of at least some of the impurities. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of the APA by using the cleaning and etching process of Doh for the purpose of obtaining a uniform thickness and a flat surface (col. 4, lines 42-44).

Regarding claim 4, Figures 2A-2F of the instant application disclose the steps of: forming a thin film transistor on the lower substrate 18; forming a protective layer 25 on the lower substrate; and forming a pixel electrode 12 on the protective layer to electrically contact the thin film transistor.

Regarding claim 5, the APA discloses the pixel electrode 12 is formed of indium-tin-oxide (page 5, para. [0013] of the instant application).

Regarding claim 6, the APA discloses the protective layer 25 is formed of an acrylic organic compound (page 5, para [0011]).

Regarding claim 7, Figures 2A-2C of the instant application disclose the step of forming the thin film transistor includes: forming a gate electrode 15 on the lower substrate 18; forming a gate insulating film 19 on the lower substrate to cover the gate electrode; forming an active layer 21 on the gate insulating film; and forming a source electrode 13 and a drain electrode 11 on the active layer.

Regarding claim 8, Figure 2C of the instant application discloses the source electrode 13 and drain electrode 11 contact the gate insulating film.

Regarding claim 9, Figure 2F of the instant application discloses the pixel electrode 12 contacts parallel and inclined surfaces of the drain electrode 11.

Regarding claim 17, Figures 2D-2F of the instant application disclose the steps of: forming a protective layer 25 on the lower substrate; and forming a pixel electrode 12 on the protective layer to electrically contact the drain electrode 11.

Regarding claim 18, the APA discloses the pixel electrode 12 is formed of indium-tin-oxide (page 5, para. [0013] of the instant application).

Regarding claim 19, the APA discloses the protective layer 25 is formed of an acrylic organic compound (page 5, para [0011]).

Response to Arguments

Applicant's arguments filed August 4, 2005 have been fully considered but they are not persuasive.

Applicant argues that Shin does not disclose the step of "cleaning exposed surfaces of the bonded upper and lower substrates to remove foreign materials form on the lower substrate during the preparing of the lower substrate". As stated in the above rejection, it is inherent that at least some type of foreign material will be formed on the lower substrate during the preparing of the lower substrate (which includes TFT formation). As also explained in the above rejection, it is inherent that at least some of the foreign material will be removed upon contact with the liquid etchant (i.e., before eliminating the surfaces of the substrate). Assuming, *arguendo*, that at least some foreign materials are not inherently removed upon contact with the liquid etchant, it is still inherent that at least some foreign materials are removed when the surface upon which they are adhered is etched away. As shown in Figures 3A-3E of Shin, a significant amount of each substrate is removed during the thinning process. Therefore, any foreign materials residing on the surface must be removed when the initial surface portions of the substrates are removed. Once the initial etching (cleaning step) removes the outermost surface of the substrate (thereby removing the foreign materials), the subsequent etching can be considered to be the "eliminating the cleaned expose surfaces" step. Applicant further argues that Shin does not disclose

“**simultaneous elimination** of cleaned exposed surfaces of the bonded upper and lower substrates”. As stated in the above rejection, Shin also discloses the exposed surfaces can be removed by immersing the bonded substrates in a liquid etchant. Therefore, it is inherent that exposed surfaces of the upper and lower substrates are eliminated simultaneously.

In response to Applicant’s arguments that Matsushima does not teach or suggest the steps of first cleaning the exposed surfaces of the bonded upper and lower substrates, and then eliminating the cleaned exposed surfaces, it is noted that the above rejection states those particular steps are inherently disclosed by Matsushima. The Examiner’s arguments presented above regarding Shin similarly apply to the rejection in view of Matsushima since both references disclose immersing the bonded substrates in a liquid etchant. It is believed that the Examiner has provided a sufficient basis in fact and/or technical reasoning to reasonable support the determination that the allegedly inherent characteristic necessarily flows from the teaching of the applied prior art. Therefore, the burden is on Applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of the claimed product (see MPEP 2112(V)). Applicant also argues that Matsushima does not disclose “eliminating cleaned exposed surfaces to prevent formation of a stain on the rear of the lower substrate and the surface of the upper substrate”. It is noted that this limitation is not found in the claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding the rejection in view of Doh, Applicant argues that since Doh discloses turning on the ultrasonic oscillator a set time after submerging the substrates in the etchant, the cleaning step of does not occur prior to the eliminating process. As stated in the above rejection, the

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etching process continues after removal of at least some of the impurities, since the etching does not stop until the substrates are removed from the etchant. Therefore, it is considered the portion of the etching process that occurs after the removal of impurity is the claimed "elimination cleaned exposed surfaces" step. Applicant also argues that Doh does not disclose "eliminating cleaned exposed surfaces to prevent formation of a stain on the rear of the lower substrate and the surface of the upper substrate". It is noted that this limitation is not found in the claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant further argues that Doh does not teach the foreign materials are formed "during preparing of the lower substrate" or "during the formation of the protective" layer as claimed. As stated in the above rejection, the APA teaches these particular limitations. Doh is merely a secondary reference relied upon for teaching the steps of cleaning foreign materials from a substrate and eliminating the cleaned exposed surfaces. The manner in which the impurities are formed in the process of Doh is not relevant to the rejection.

Allowable Subject Matter

Claims 2, 11, and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, either singularly or in proper combination, does not disclose or suggest the

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combination of limitations including the step of cleaning the exposed surfaces includes dry-etching. Note that although Yoshida discloses using a dry-etch to remove organic impurities from a substrate, the reference does not appear to disclose performing any further processing of the substrate after the etching step. Therefore, there is no motivation to perform a dry-etching step prior to the surface removal step disclose by the APA.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

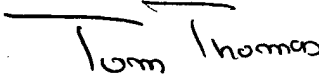
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached

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on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


TOM THOMAS
SUPERVISORY PATENT EXAMINER

Matthew C. Landau

October 27, 2005